REMARKS

In the final Office Action, dated October 20, 2004, the Examiner has rejected claims 1-6, 8-32 and 41-46, and has allowed claims 33-40. Applicants acknowledge and appreciate the Examiner's statement regarding allowance of claims 33-40. By the present amendment, claims 15-32 and 41-43 have been cancelled. After the present amendment, claims 1-6, 8-14, 33-40 and 44-46 remain pending in the present application. Reconsideration and allowance of pending claims 1-6, 8-14 and 44-46 in view of the following remarks are requested.

A. Rejection of Claims 1-2, 4-6, 8-32, and 41-46 Under 35 USC §102(e)

The Examiner has rejected claims 1-2, 4-6, 8-32, and 41-46 under 35 USC §102(e) as being anticipated by U.S. Patent Number 6,597,394 to Duncan, et al. ("Duncan"). For the reasons discussed below, Applicants respectfully submit that independent claims 1, 13, 14, 44, and 46 are patentably distinguishable over Duncan.

In accordance with one embodiment at page 25, lines 18-22, the present application reads as follows:

> As shown in the example of FIG. 7B, for video processing or other real-time data stream, the buffers of level zero and level one are alternately used for fetching input image data, while the buffers of level two and level three are alternately used for storing output image data. In this way, image data is input, processed and output in every cycle.

FIG. 7B illustrates phases zero, one, two and three of a timing diagram in conjunction with the operation of buffers 500 of level zero, one, two and three. As shown, in phase zero, block0 of the image data is loaded into the level zero buffer. In phase one, block0 of the image data is read from the level zero buffer and stored into the level two buffer; and block1 of the

image data is loaded into the level one buffer. In phase two, block2 of the image data is loaded into the level zero buffer; and block1 of the image data is read from the level one buffer and stored into the level three buffer. In phase three, block2 of the image data is read from the level zero buffer and stored into the level two buffer; and block3 of the image data is loaded into the level one buffer.

With reference to FIG. 7B, it is shown that level zero buffer and level one buffer are alternately used to read (or load) input image data, and level two buffer and level three buffer are alternately used to store output image data.

Turning to the Examiner's rejection of claim 1 and the Examiner's response to Applicants' arguments, the Examiner states that FIG. 6A of Duncan shows that each buffer in the first set of local buffers (latches 640-643) are alternately used for fetching input image data, and each buffer in the second set of local buffers (latches 646-647) are alternately used for storing output image data. Applicants respectfully disagree with the Examiner's statement. Applicants respectfully submit that FIG. 6A and its related written description at Col. 14, line 66 through Col. 15, line 67, fail to disclose, teach or suggest that latches 640-643 are used "alternately" for fetching input image data and/or latches 646-647) are used "alternately" for storing output image data. In fact, Duncan states that "The output of a pair of latches, i.e. latches 640 and 641, and latches 642 and 643 is supplied to adders 644, 645 respectively. The out put of the adders 644 and 645 is supplied to latches, 646, 647, respectively." (Col. 15, lines 48-50.) Therefore, there is no support for the Examiner's assertion that latches 640-643 are used "alternately" for fetching the input image data, and/or latches 646-647 are used "alternately" for storing the output image data.

Accordingly, applicants respectfully submit that claim 1 is patentably distinguishable over Duncan and should be allowed. In addition, claims 2, 4-6 and 8-12 depend from claim 1, and should be allowed at least for the same reason stated above in conjunction with patentability of claim 1. Furthermore, independent claims 13, 14, 44 and 46 include limitations similar to those described above in conjunction with patentability of claim 1 and, thus, claims 13, 14, 44 and 46 should be allowed at least for the same reason stated above in conjunction with patentability of claim 1. Also, claim 45 depends from claim 44, and should be allowed at least for the same reason stated above in conjunction with patentability of claim 1.

B. Rejection of Claim 3 under 35 USC §103(a)

The Examiner has rejected claim 3 under 35 USC §103(a) as being unpatentable over Duncan in view of U.S. Patent Number 6,100,928 to Hata ("Hata").

First, Applicants respectfully submit that, according to 35 USC § 103(c), the Duncan patent does not qualify as a prior art reference for the purpose of a rejection under 35 USC § 103(a). 35 USC § 103(c) reads as follows:

> Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. (emphasis added.)

Applicants respectfully submit that the Duncan patent, and the subject matter and the claimed invention of the present application was, at the time the invention of the present application was made, owned by Conexant Systems, Inc. or subject to an obligation of assignment to Conexant Systems, Inc. Therefore, the Duncan patent cannot be considered a prior

art reference for the purpose of rejecting claims of the present application under 35 USC § 103(a).

Furthermore, Applicants respectfully submit that claim 3 depends from amended independent claim 1, and thus, claim 3 should be allowed at least for the same reasons discussed above in conjunction with patentability of amended independent claim 1.

C. Conclusion

For all the foregoing reasons, an early Notice of Allowance for claims 1-6, 8-14, 33-40 and 44-46 pending in the present application is respectfully requested.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 11/5/04

Farshad Farjami
Reg. No. 41,014

FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Telephone: (949) 282-1000
Facsimile: (949) 282-1002

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service "First Class Mail Post Office to addressee" under 37 C.F.R. Sec. 1.10 addressed to: Commissioner for Patents. P. O. Box 1450. Alexandria, VA 22313-1450, on 11/5/04.

Christina Carter
Name

Christina Carter
Signature